ABSTRACT OF THE DISCLOSURE

A method and apparatus for performing a memory built-in self-test for an integrated circuit are disclosed. The technique includes a memory built-in self-test controller including a plurality of alternative memory built-in self-test state machines and a memory built-in self-test engine operating a predetermined one of the memory built-in self-test state machines. It also includes a method for performing a built-in self-test on an integrated circuit device. The method includes externally resetting a predetermined one of a plurality of memory state machines in a memory built-in self-test controller; performing a memory built-in self-test utilizing the reset memory state machine ; and obtaining the results of the performed memory built-in self-test.